Amendments to the Specification:

Please replace the paragraph starting on page 7, line 6, with the following amended paragraph:

FIG. 10 shows a schematic circuit diagram of a multi-stage buffer circuit, wherein n-well and p-well bias voltages VNW and VPW can be controlled to change the threshold voltage of individual transistor elements or other semiconductor elements. The control of the bias voltages leads to the advantage that a smaller buffer circuit with lower power-delay-product (PDP) compared to conventional buffers can be achieved at identical or faster speed for all ranges of load from as small as 10 fF up to 2.75 pF. FIG. 10 includes a line 52, a line 54, an input 100, a line 102, a line 104, a line 106, an output 108, a first group of transistors 110, and a second group of transistors 112. Line 52 carries the p-well bias voltage VPW. Line 54 carries the n-well bias voltage VNW. Line 52 connects the control circuit 50 to the body of each transistor on the bottom rows of the transistors in the first and second group of transistors 110 and 112. Line 54 connects the control circuit 50 to the body of each transistor on the top rows of the transistors in the first and second group of transistors 110 and 112. Line 102 connects an input 100 to the gates of each of the transistors in the first group of transistors 110. Line 104 connects the drains of the first group of transistors 110 to the gates of each of the transistors in the second group of transistors 112. Line 106 connects the drains of the second group of transistors 112 to an output 108.